TH24C64UA

Ultra Low Power, 64K-bit

I2C-Compatible Serial EEPROM Datasheet

Apr, 2021

V1.1

Performance Highlight

- *Wide Power Supply Range from 1.7V to 5.5V*
- *Ultra Low Power consumption for Read and Program*
- *High ESD Protection and Latch up Capability*
- *High reliability with 1000K cycling and 100 Years data retention*

Contents

General Description

The TH24C64UA is 64-Kbit I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. The device is organized as 8192 × 8bits memory array with 32- byte per page. TH24C64UA provides the following features for different application.

Features

Compatible with IIC bus modes
- ✧ 1 MHz clock from 2.5V to 5.5V
- ✧ 400KHz clock from 1.7V to 2.5V

Wide Supply Voltage and temperature
- ✧ operating voltage from 1.7V to 5.5V
- ✧ operating temperature from -40 °C to 85 °C

Low power CMOS technology
- ✧ Read current 400μA, maximum
- ✧ Write current 2mA, maximum

Schmitt Trigger, Filtered Inputs for Noise Suppression

Memory array
- ✧ 64 Kbits (8 Kbytes) of EEPROM
- ✧ Page size: 32 bytes
- ✧ Additional Write Lockable Page and 128-bit Serial Number

Sequential & Random Read Features

Page Write Mode, Partial Page Writes Allowed

Write protection of the whole memory array

Self-timed Write Cycle (5ms maximum)

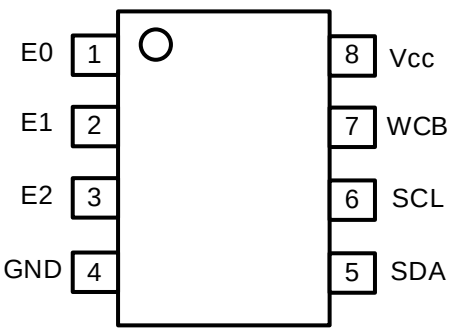
High Reliability
- ✧ Endurance: 1 Million Write Cycles
- ✧ Data Retention: 100 Years
- ✧ ESD Protection (HBM): +/- 5KV
- ✧ Latch up Capability: +/- 200mA (25°C and 125°C)

Package: PDIP-8, SOP-8, TSSOP-8, MSOP-8, DFN-8/UDFN-8, SOT23-5, TSOT23-5, WLCSP-4

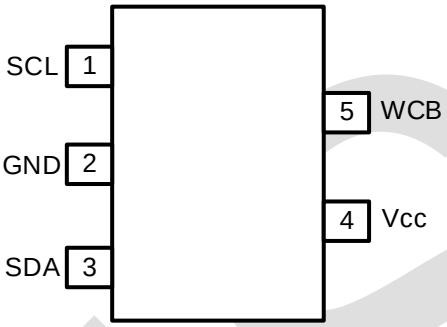
1. Pin Configuration

1.1 Pin Configuration

Figure 1-1 8 Pin and 5 Pin Configuration



PDIP-8/TSSOP-8/
SOP-8/DFN-8/MSOP-8



SOT23-5/TSOT23-5

1.2 Pin Definition

Table 1-1 Pin Definition for PDIP-8/SOP-8/TSSOP-8/DFN-8/MSOP-8 Packages

Pin	Name	Type	Description
1	E0	Input	Slave Address Setting Bit0
2	E1	Input	Slave Address Setting Bit1
3	E2	Input	Slave Address Setting Bit2
4	GND	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	Vcc	Power	Power Supply

Table 1-2 Pin Definition for SOT23-5/TSOT23-5 Packages

Pin	Name	Type	Description
1	SCL	Input	Serial Clock Input
2	GND	Ground	Ground
3	SDA	I/O	Serial Data Input and Serial Data Output
4	Vcc	Power	Power Supply
5	WCB	Input	Write Control, Low Enable Write

1.3 Pin Descriptions

Serial Clock (SCL): The SCL is input pin. It is used to clock in data at positive edge and clock out data from EEPROM at negative edge.

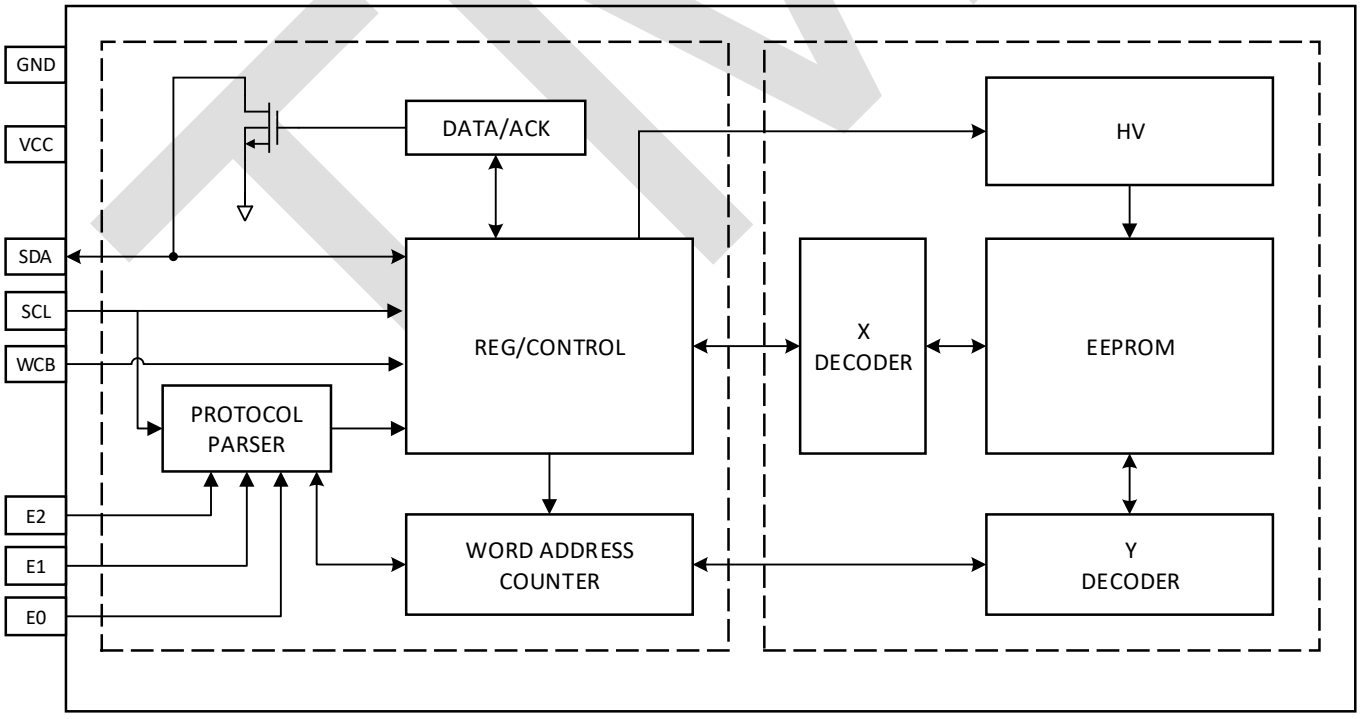
Serial Data (SDA): The SDA is bidirectional for serial data transfer. This pin is open drain driven and may be wired AND with any number of other open-drain or open-collector devices. The SDA requires a pull-up device connected to the power supply.

Device address (E2, E1, E0): The E2, E1 and E0 pins are chip enable inputs of device address. Typically, the E2, E1 and E0 pins need hardware addressing and eight devices at most can be connected on a single bus system. If E2, E1 and E0 are left floating, they will be internally pulled down to logic 0, and the corresponding device address is set to 0.

Write Control (WCB): This input signal is used for protecting the entire contents of the EEPROM from inadvertent write operations. All write operations are disabled when Write Control (WCB) is driven high. All write operations are enabled when Write Control (WCB) is either driven low or left floating.

2. Block Diagram

Figure 2-1 Block Diagram



3. Electrical Characteristics

Table 3-1 Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Units
T	Operation Temperature	-40	85	°C
T_{STG}	Storage Temperature	-55	150	°C
V_M	Maximum Operation Voltage	-0.3	5.8	V
I_{OLM}	DC Output Current		5	mA

NOTICE: Stressing the device outside the ratings listed in Table 3-1 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3-2 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$=GND
C_{IN}	Input Capacitance (E0, E1, E2, WCB, SCL)	6	pF	V_{IN}=GND

Note: [1] Test Conditions: T_A = 25°C, Freq. = 1MHz, Vcc =5.5V.

Table 3-3 DC Characteristics （Unless otherwise specified, Vcc = 1.7V to 5.5V, T_A = –40°C to 85°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
Vcc	Supply Voltage	1.7	-	5.5	V	
Isb	Standby Current		2.5	15	μA	Vcc = 5.5V
I_{CC1}	Supply Current	-	0.2	0.4	mA	Vcc = 5.5V, Read at 400Khz
I_{CC2}	Supply Current	-	1.0	2.0	mA	Vcc = 5.5V Write at 400Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = Vcc or GND
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = Vcc or GND
V_{IL}	Input Low Level	–0.6	-	0.3Vcc	V	
V_{IH}	Input High Level	0.7Vcc	-	Vcc+0.5	V	
V_{OL1}	Output Low Level Vcc = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level Vcc = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA
Rpd	Pull-down resistance on WCB	5	50		MΩ	V_{IN} = Vcc
		10	30		KΩ	V_{IN} < V_{IL}

Table 3-4 AC Characteristics （Unless otherwise specified, Vcc = 1.7V to 5.5V, T_A = –40°C to 85°C, C_L=100pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤Vcc<2.5			2.5≤Vcc≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.5	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.4	μs
t_I	Noise Suppression Time	-	-	0.08	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	START Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	START Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	STOP Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	μs
$t_{HD.WCB}$	WCB pin Hold Time	1.2	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- ✧ R_L (connects to Vcc): 1.3kΩ (2.5V, 5.5V), 4kΩ (1.7V)
- ✧ Input pulse voltages: 0.3 Vcc to 0.7 Vcc
- ✧ Input rise and fall times: ≤50ns
- ✧ Input and output timing reference voltages: 0.5Vcc

Table 3-5 Reliability Characteristics [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C/ 85°C, 5.5V, Page mode

Figure 3-1 Bus Timing

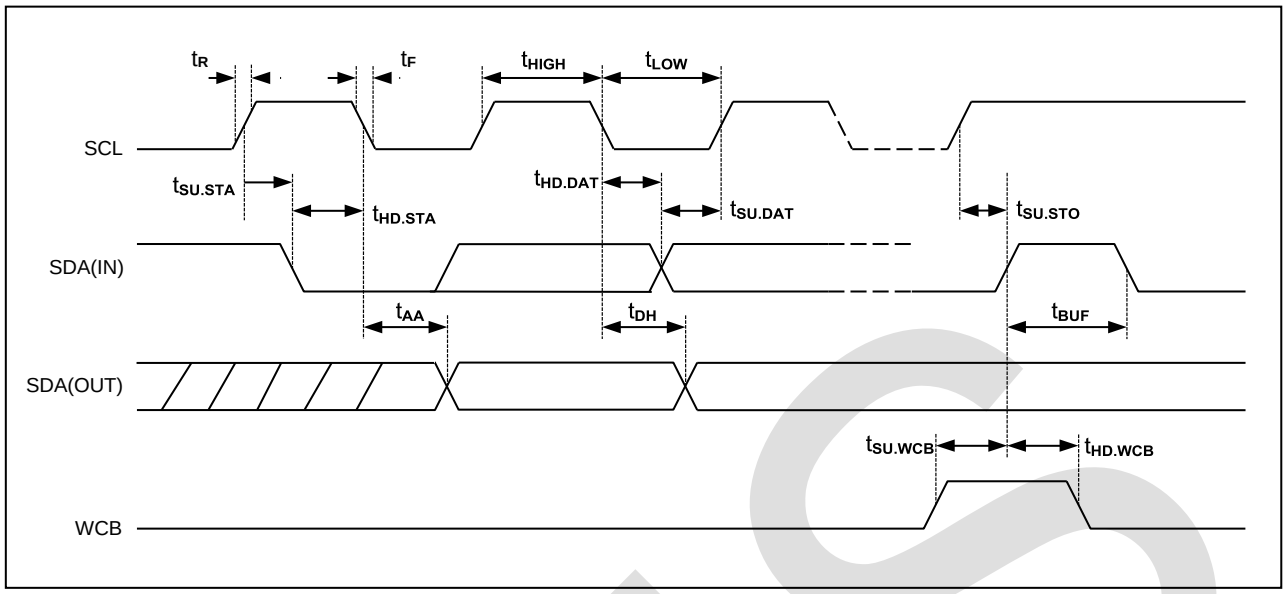
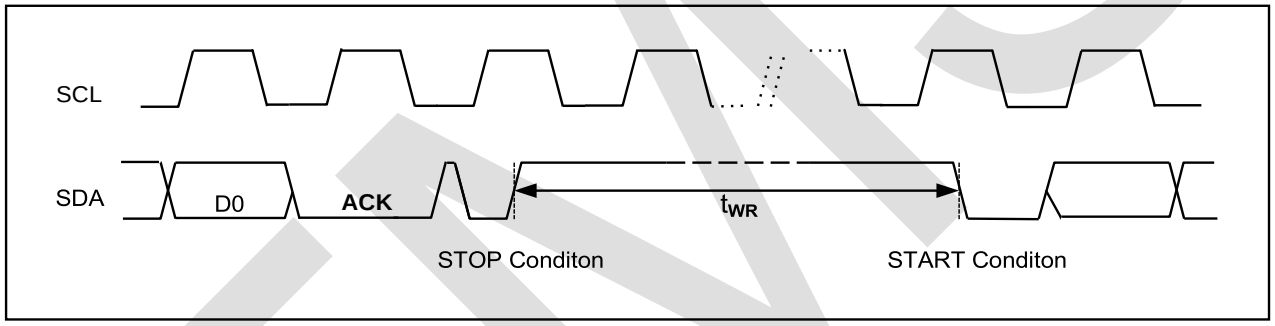


Figure 3-2 Write Cycle Timing



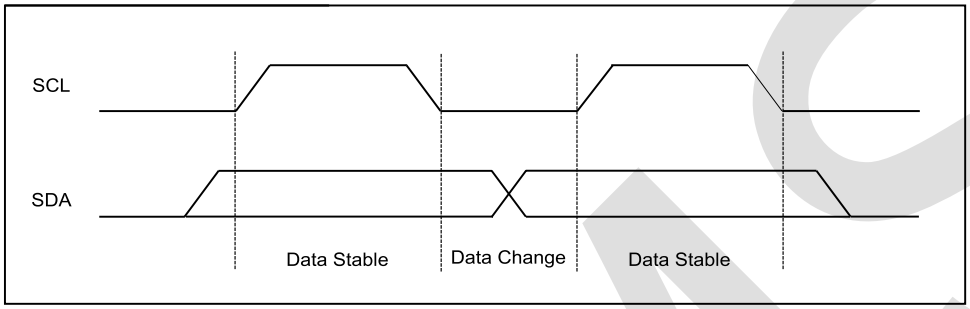
Note: [1] The write cycle time t_{WR} is the time from a valid STOP condition of a write sequence to the end of the internal clear/write cycle.

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high by an external device. Data on the SDA pin may change only during SCL low period (Refer to Figure 4-1). Data changes during SCL high period will indicate a START or STOP condition as defined below.

Figure 4-1 Data Validity



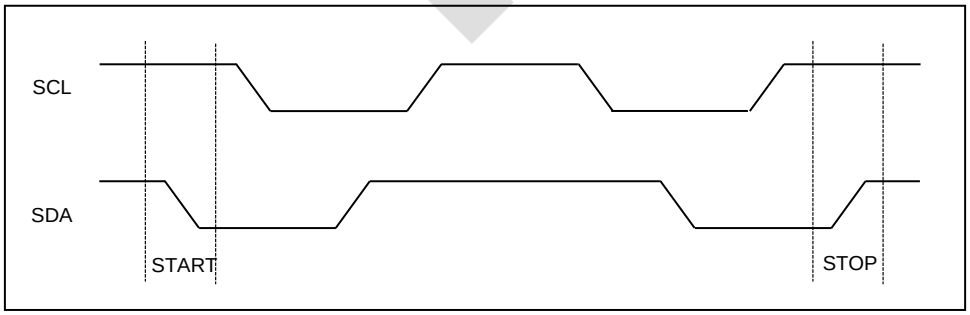
4.2 START Condition

A high-to-low transition on SDA while SCL high is a START condition, the START condition must precede any other command bits. (Refer to Figure 4-2).

4.3 STOP Condition

A low-to-high transition of SDA with SCL high is a STOP condition. After a read sequence, the STOP bit will place the TH24C64UA in a standby mode (Refer to Figure 4-2).

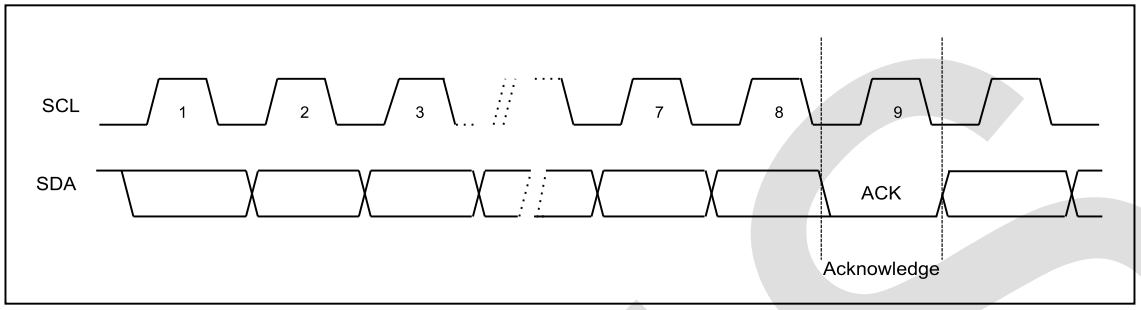
Figure 4-2 START and STOP Definition



4.4 Acknowledge (ACK)and Not Acknowledge (NoACK)

All addresses and data should be serially transmitted to and from the TH24C64UA by byte. Each byte must be 8-bit long. The TH24C64UA sends a “0” to acknowledge (ACK) that it has received each data. An ACK means SDA pull down during the ninth clock cycle. A NoACK means SDA pull up during the ninth clock cycle.

Figure 4-3 Acknowledge Bit Definition



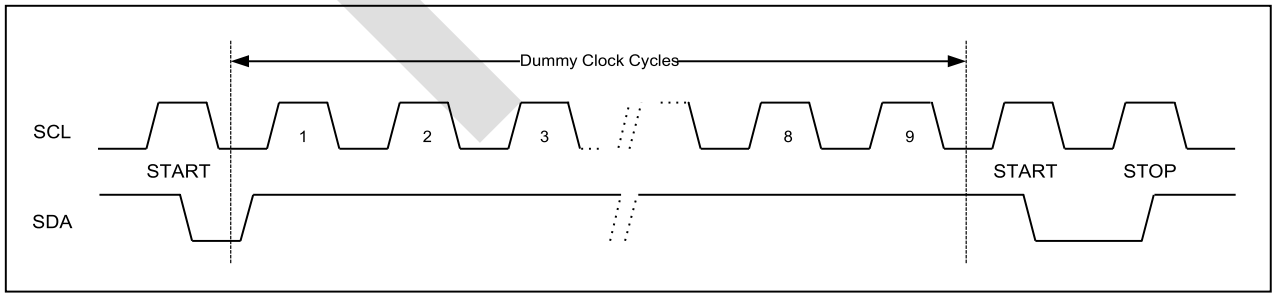
4.5 Standby Mode

The TH24C64UA features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP condition in read mode, and (c) after completing a self-time internal programming operation.

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, the device can be reset by following steps: (a) Create a START condition, (b) Clock in nine data bits “1”, and (c) create another START condition followed by a STOP condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.7 Device Address

The TH24C64UA requires an 8-bit device address after a START condition to enable the chip, the 8-bit device address consists of a 4-bit device type identifier and a 3-bit Chip Enable address (E2, E1, E0). Refer to table below:

Table 4-1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH24C64UA	Normal Area	1	0	1	0	E2	E1	E0	R/W
	ID Page	1	0	1	1	E2	E1	E0	R/W
	Lock Bit	1	0	1	1	E2	E1	E0	R/W
	Serial Number	1	0	1	1	E2	E1	E0	1

Table 4-2 Word Address0

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH24C64UA	Normal Area	X	X	X	A12	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	X	1	X	X
	Serial Number	X	X	X	X	1	0	X	X

Table 4-3 Word Address1

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH24C64UA	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	X	X	A5	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	Serial Number	X	X	X	X	A3	A2	A1	A0

The E2, E1 and E0 bits allow at most eight devices on the same system bus. These bits must compare to their corresponding hardwired input pins. The E2, E1 and E0 pins will be put a logic low condition by inner circuit if these pins are left floating. The bit0 of the device address is the read/write operation selection bit. If bit0 is high, A read operation is initiated, if bit0 is low, a write operation is initiated. Upon a matched comparison result, the device will output a ACK. If not, the device will return to a standby state.

4.8 Data Security

TH24C64UA has a hardware data protection scheme. when WCB is high, all write operations are disabled, users can protect the whole chip.

5. Instructions

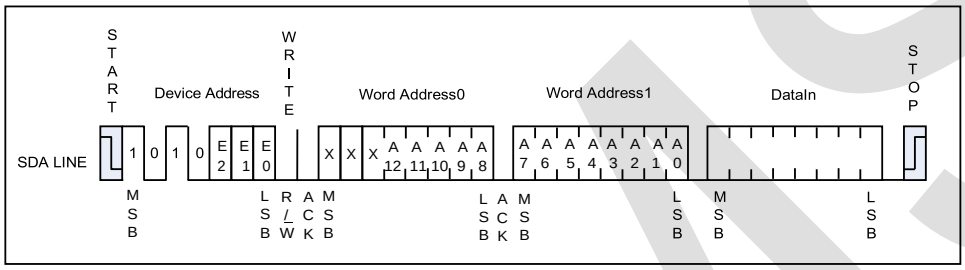
5.1 Write Operations

The read/write selection bit of Write Operations in the device address is “0”. There are two write operations: Byte Write and Page Write. In addition, Write Operations is corresponding to some utilities.

5.1.1 Byte Write

Byte write operation requires one-byte device address, two-byte word address and one-byte data in order. After receiving each byte, the device will respond an ACK. The master must terminate the write sequence with a STOP condition. And then the TH24C64UA enters an internally timed write cycle. All inputs are blocked during this write cycle and the TH24C64UA will not respond until the write is complete (Refer to Figure 5-1).

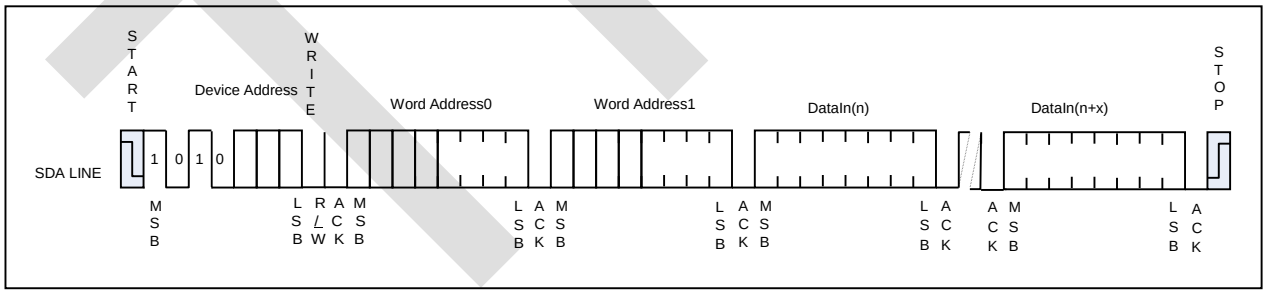
Figure 5-1 Byte Write



5.1.2 Page Write

Page write performs a similar way to Byte Write. The difference is that Page Write will not generate a STOP condition after clock in the first byte. Instead, after the TH24C64UA acknowledges receipt of the first byte data, the master can transmit more data continuously. The TH24C64UA will respond with a “0” after each data byte received. The master must terminate the page write sequence with a STOP condition (Refer to Figure 5-2).

Figure 5-2 Page Write



The lowest five bits of the word address are internally incremented by one. The higher word address bits stay constant, retain the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 bytes data are transmitted to the TH24C64UA, the word address will roll-over and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started, the TH24C64UA inputs are blocked, will not respond any ACK. To find out whether this cycle is over, Acknowledge Polling could be used. This involves sending a START condition followed by the device address. The read/write bit is representative of the desired operation. Until the internal write cycle has completed, TH24C64UA will response “0”, allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (refer to 5.1.2), except for the following differences:

- Device type identifier = 1011b
- Address bits A11/A10 must be ‘00’.
- Address bits A4~A0 define the byte address inside the Identification page.
- Other Address bits are don’t care.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.1.5 Lock Identification Page

The Lock Identification Page (Lock ID) instruction permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (refer to 5.1.1), except for the following differences:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

5.2 Read Operations

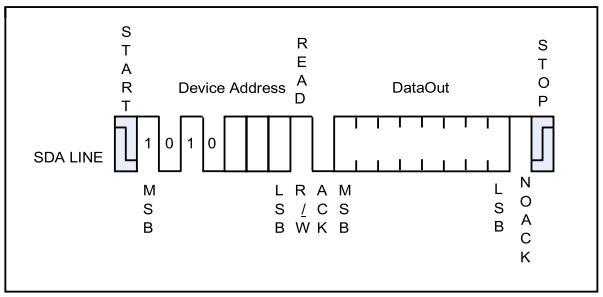
Read operations are initiated in the same way as write operations, except the read/write selection bit in the device address is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

If the power is stay valid, After the STOP condition of the last command, the last address accessed during the last read or write operation is always incremented by one, For the Current Address Read operation, following a START condition, the bus master only sends device address with the R/W selection bit 1. The device acknowledges this, the data at the current address (the last address accessed during the last read or write operation incremented by one) is serially clocked out. The master can send a NoACK and a STOP condition to terminate the Current Address Read. (Refer to Figure 5-3).

If the last byte of the last memory page is reached, the address counter rolls over to the first byte of the first page.

Figure 5-3 Current Address Read

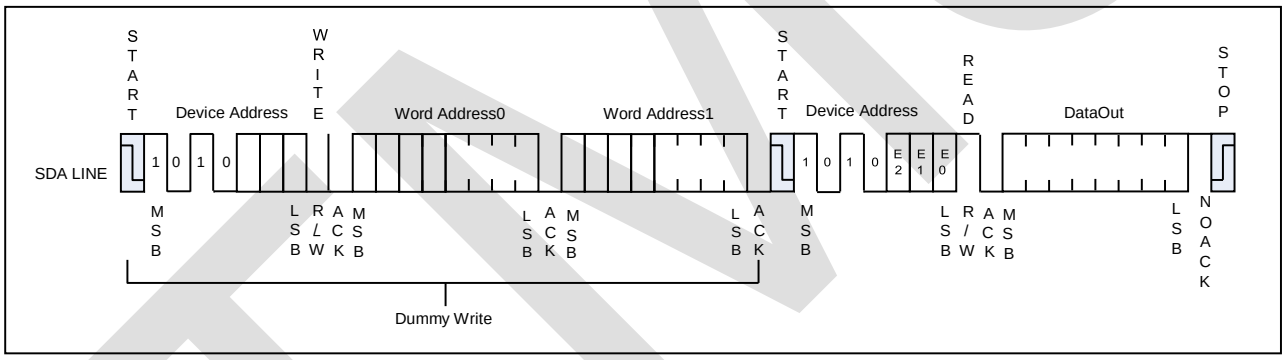


5.2.2 Random Read

The Random Address Read is a sequence composed of a truncated Write sequence (to define a new address pointer value) followed by a current Read.

The Random Address Read sequence is therefore the sum of [START + Device Address with R/W=0 + two address bytes] (without STOP condition) and [START + Device Address with R/W=1]. The memory device acknowledges the sequence and then outputs the contents of the addressed byte. To terminate the data transfer, the bus master does not acknowledge the last data byte and then issues a STOP condition. (Refer to Figure 5-4).

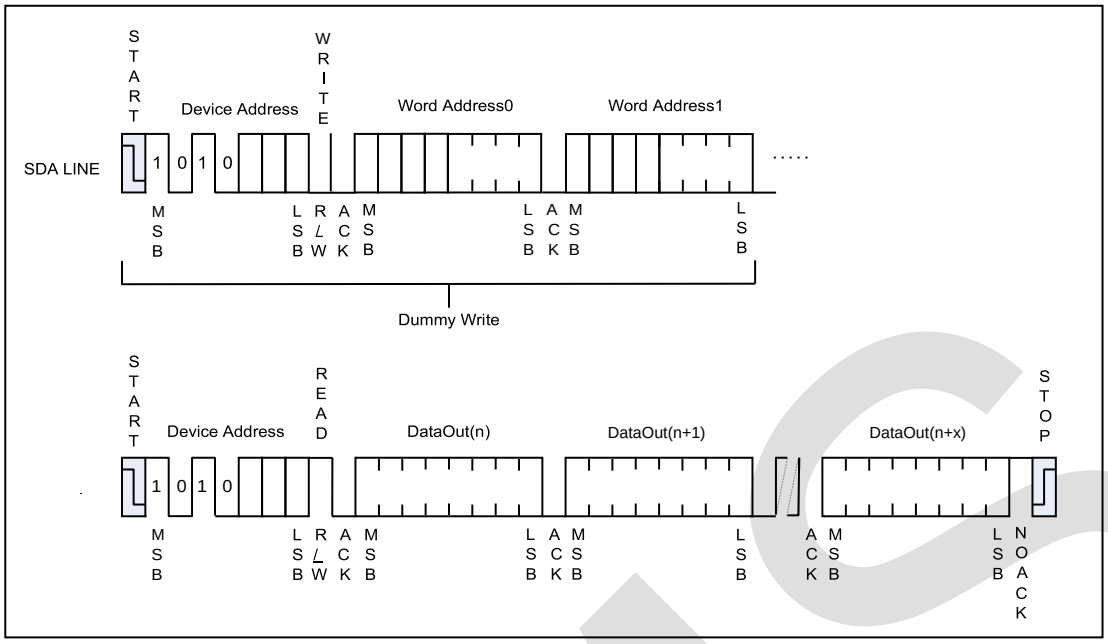
Figure 5-4 Random Read



5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the master receives a byte data, it responds with an ACK. As long as the device receives ACK, it will continue to increment the word address and serially clock out the reading data. When the memory address boundary is reached, the word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the master does not respond with a “0” and following a STOP condition. (Refer to Figure 5-5)

Figure 5-5 Sequential Read



5.2.4 Read Identification Page

The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (refer to 5.2.3), except for the following differences:

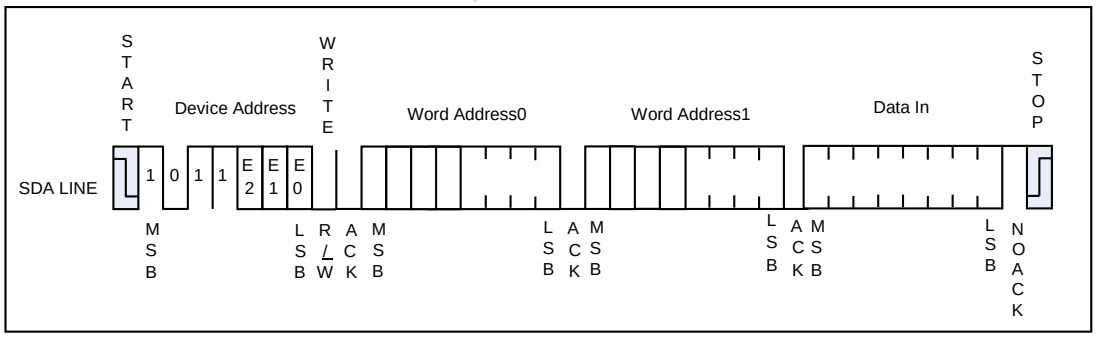
- Device type identifier = 1011b.
- The word address bits A11 and A10 must be 0.
- The LSB address bits A4~A0 define the byte address inside the Identification Page.

The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 28d, the number of bytes should be less than or equal to 4, as the ID page boundary is 32 bytes).

5.2.5 Read the Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific command sequence [Identification Page Write instruction + one data byte] to the device. The device returns an ACK if the Identification page is unlocked or a NoACK if the Identification page is locked. (Refer to Figure 5-6)

Figure 5-6 Lock Status Read (When Identification page locked, return No-ACK after the data-in)



5.2.6 Read Serial Number

The serial number is an additional unique 128 bits which can be read only.

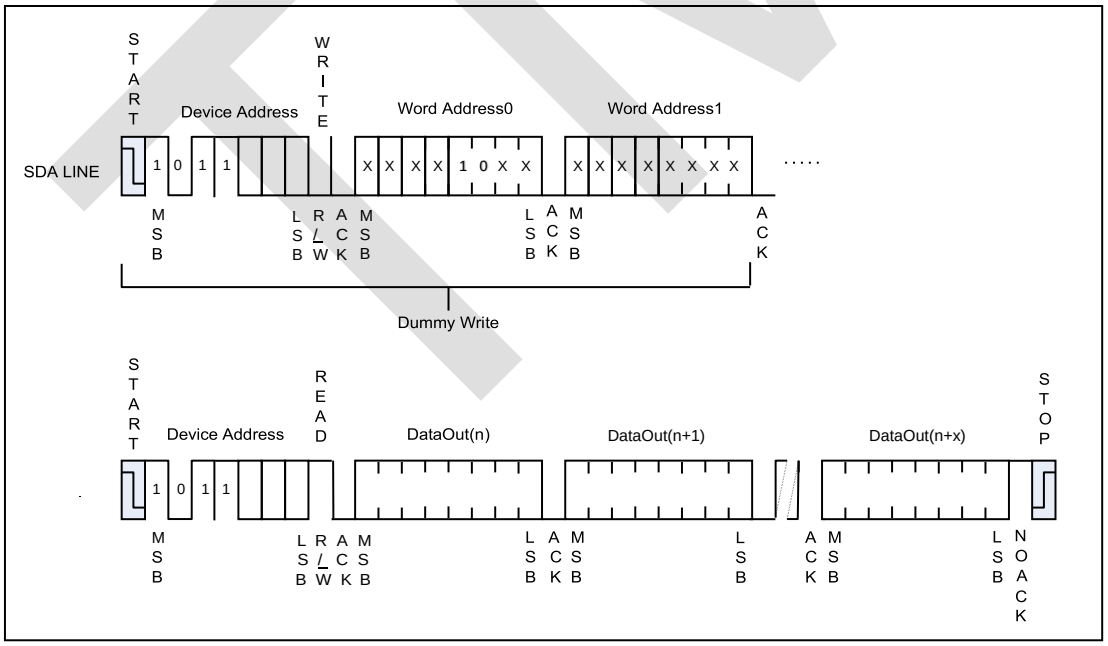
Reading the serial number is similar to the sequential read scheme, but the device address must follow Table 4-1, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number region to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number region, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one.

Additionally, bit A11 and A10 of Word Address must be '10', refer to the Table 4-2. If a Word Address other than '10' is used, then the device will output undefined data.
Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

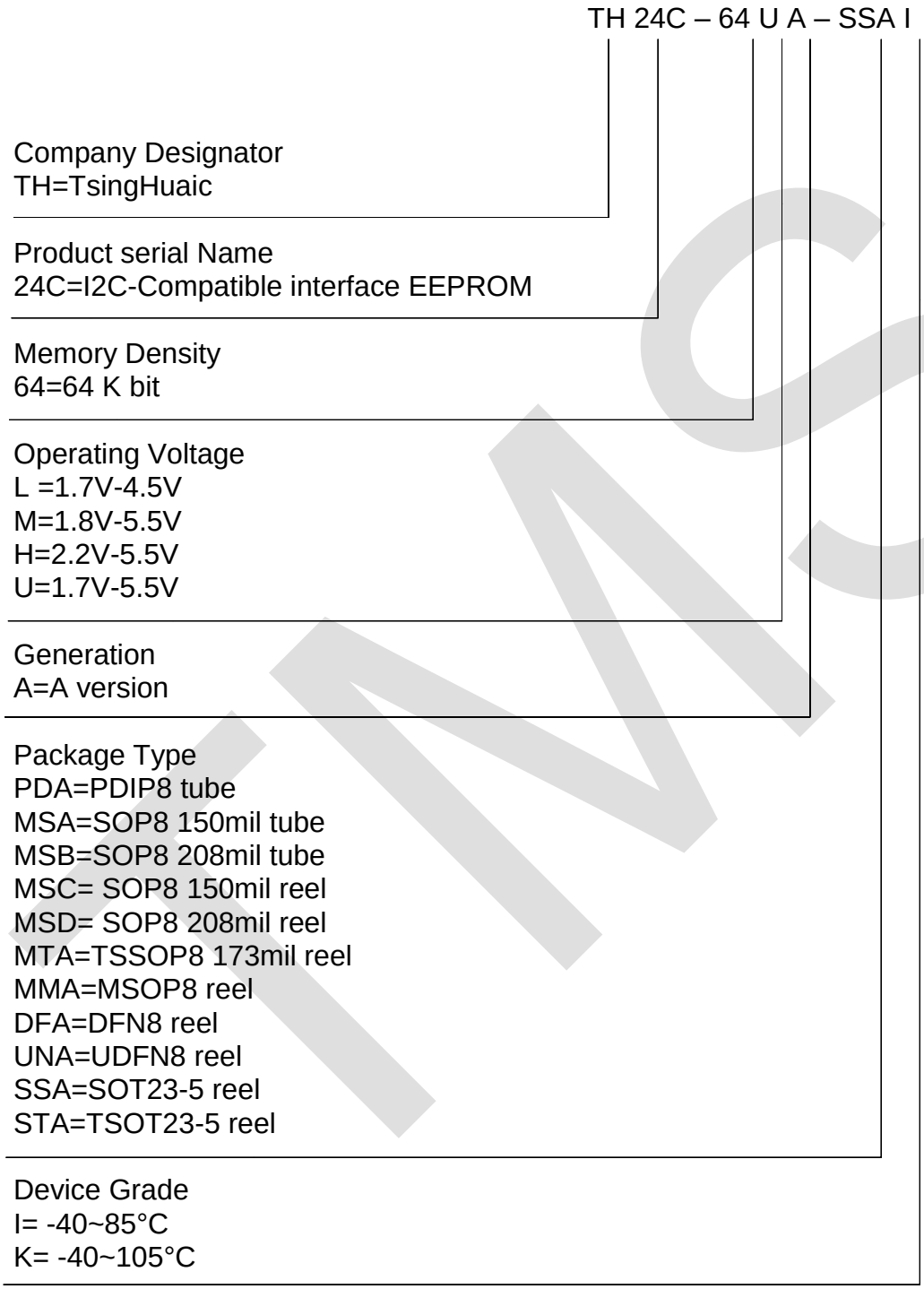
When the end of the 128-bit serial number is reached (16 bytes of data), continue reading the extended memory region will result in a repeated 16 bytes data. Upon reaching the end of the 16-byte extended memory region, the word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the master does not respond with a zero (ACK) and instead issues a STOP condition (Refer to Figure 5-7)

Figure 5-7 Sequential Read



6. Ordering Code Detail

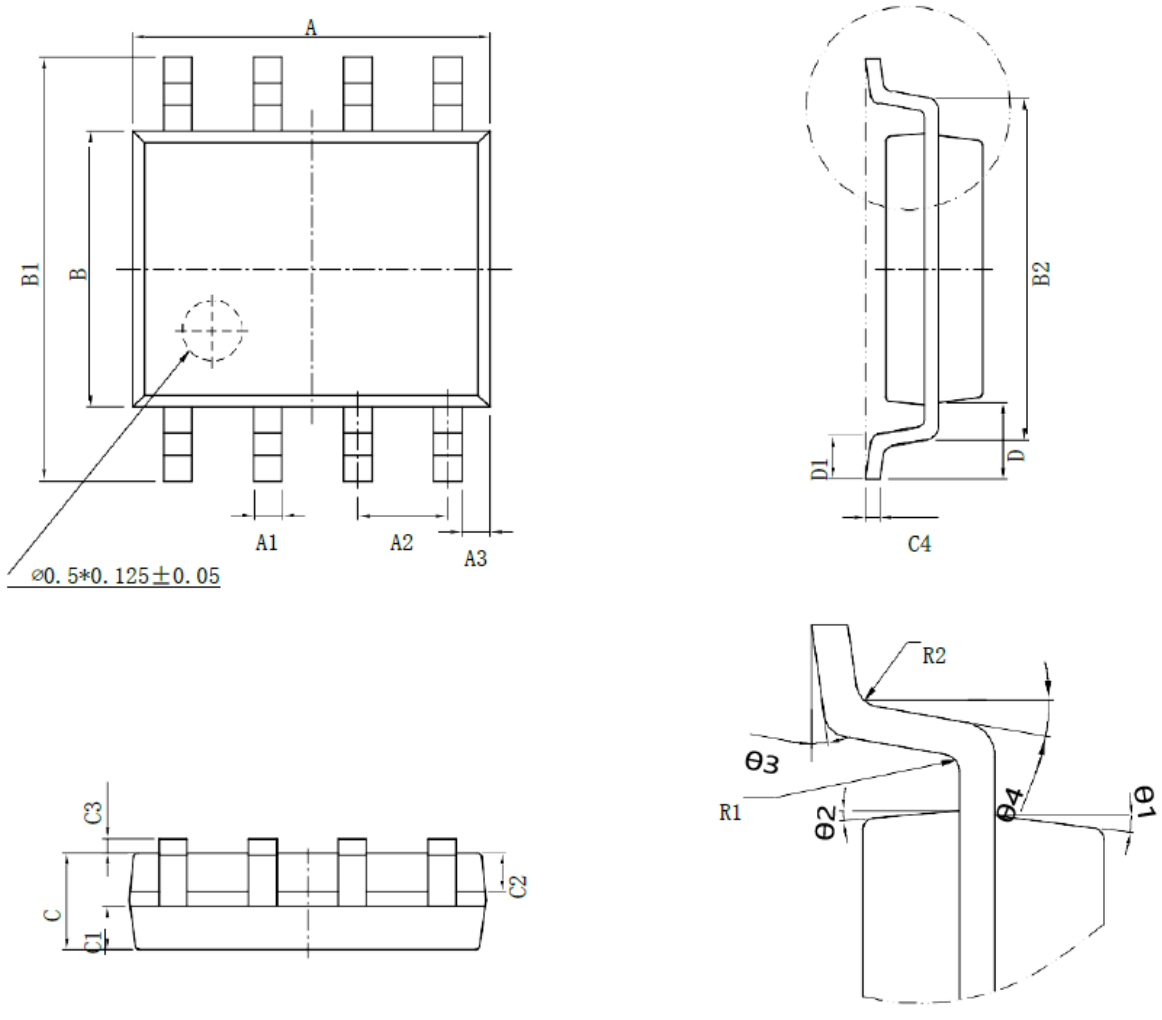
Example:



7. Package information

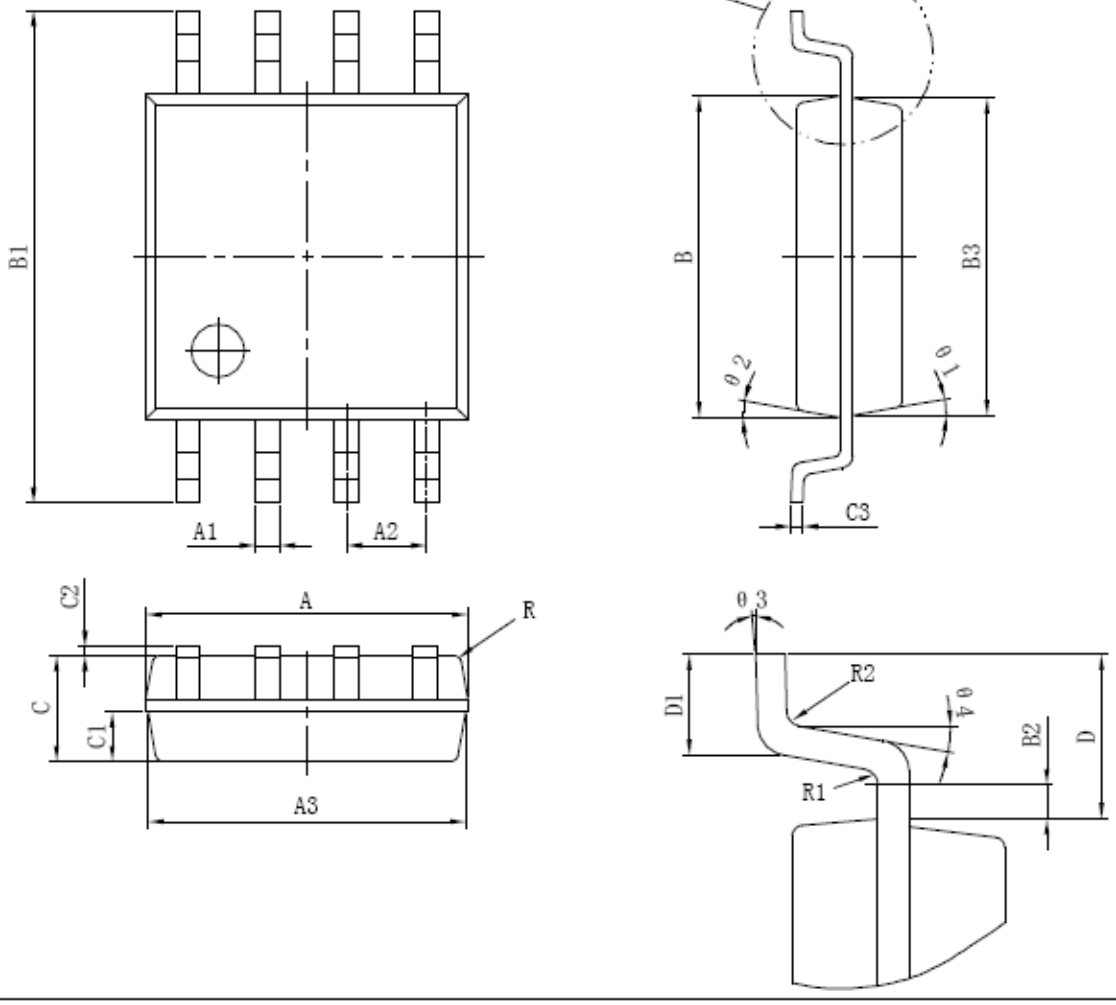
7.1 8-lead SOP(150mil)

Symbol \ size	min(mm)	max(mm)	symbol \ size	min(mm)	max(mm)
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	1.05TYP	
A3	0.345TYP		D1	0.40	0.80
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
B2	5.00TYP		θ1	17° TYP4	
C	1.30	1.60	θ2	13° TYP4	
C1	0.55	0.65	θ3	0° ～ 8°	
C2	0.55	0.65	θ4	4° ～ 12°	



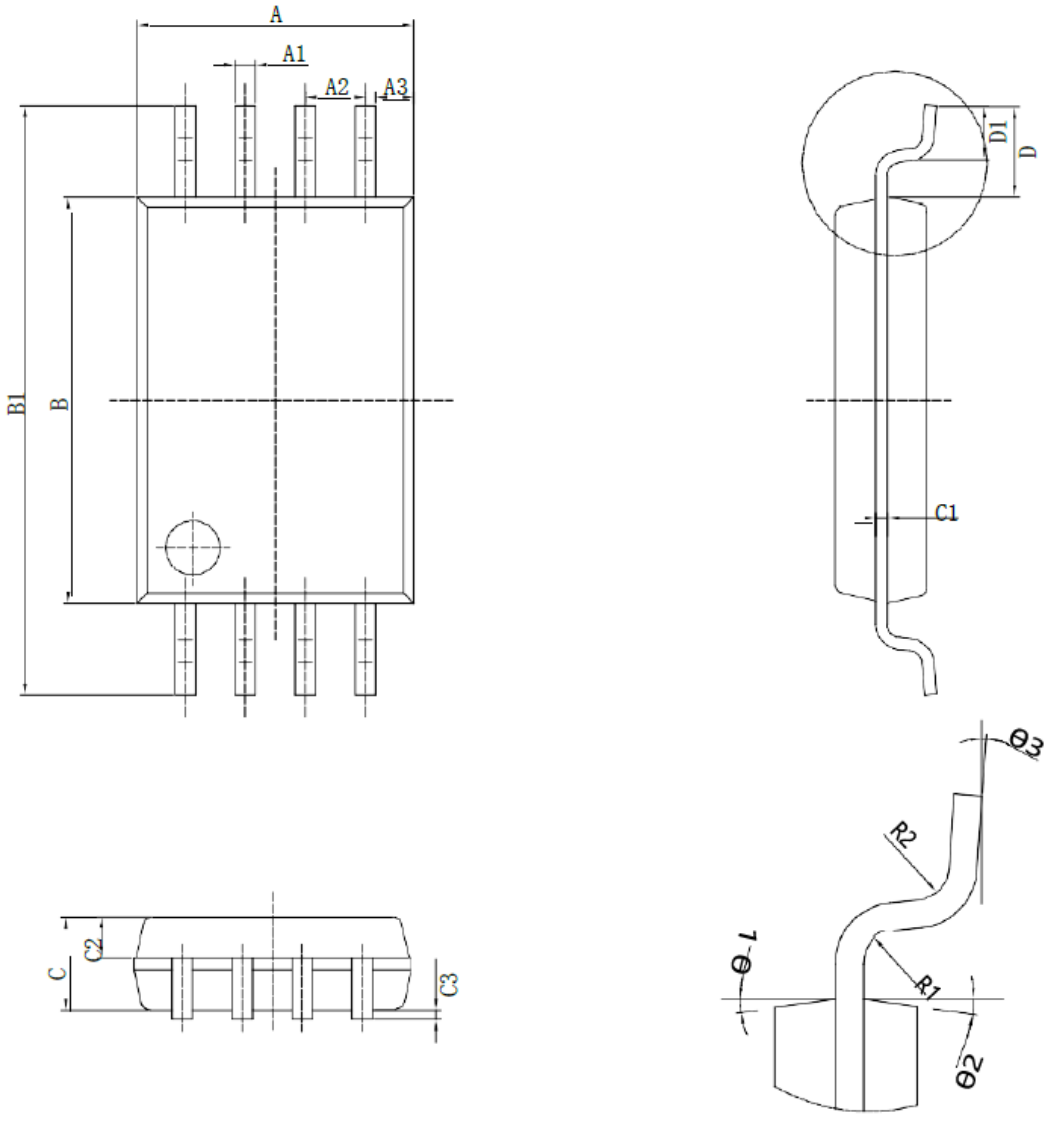
7.2 8-lead SOP(208mil)

Symbol \ size	min(mm)	max(mm)	symbol \ size	min(mm)	max(mm)
A	5.13	5.33	C3	0.203REF	
A1	0.38	0.48	D	1.31REF	
A2	1.27REF		D1	0.50	0.80
A3	5.12	5.22	R	0.127TYP8	
B	5.18	5.38	R1	0.20REF	
B1	7.70	8.10	R2	0.20REF	
B2	0.35	0.40	θ1	10° TYP4	
B3	5.17	5.27	θ2	10° TYP4	
C	1.70	1.90	θ3	2° ~ 6°	
C1	0.848	0.948	θ4	3° ~ 7°	
C2	0.05	0.15			



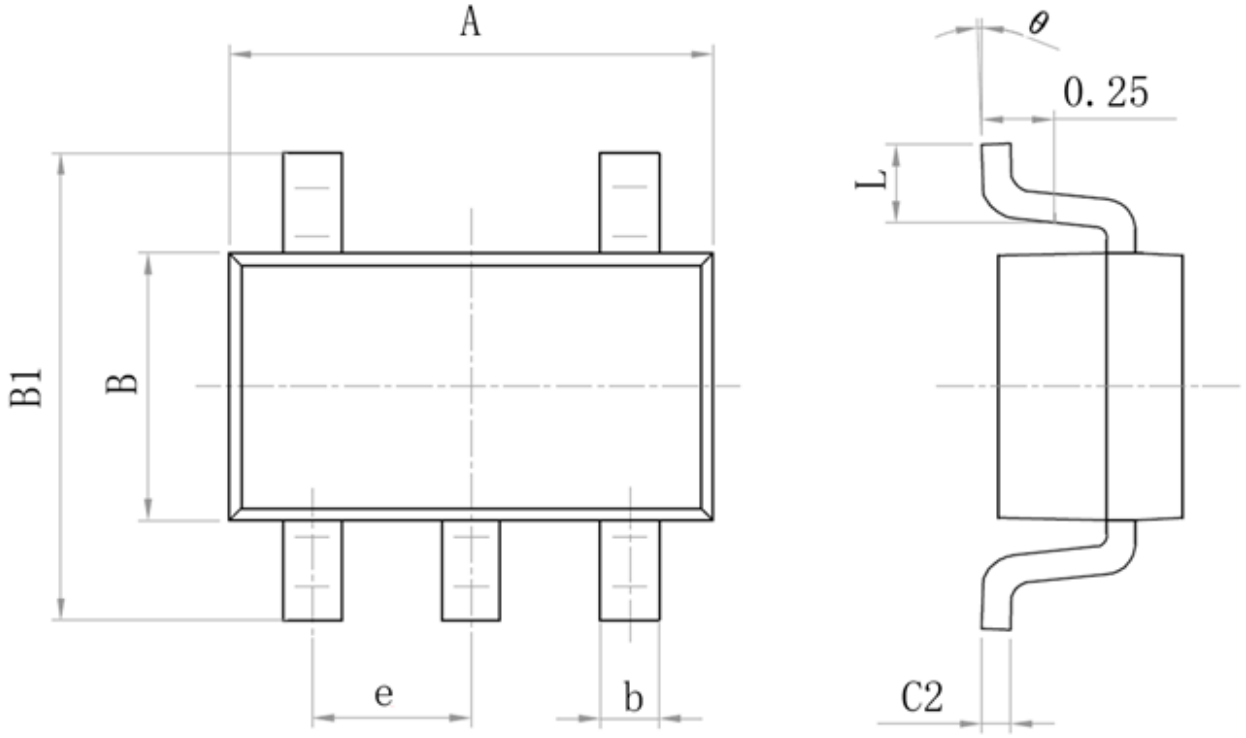
7.3 8-lead TSSOP8(173mil)

size / symbol	min(mm)	max(mm)	size / symbol	min(mm)	max(mm)
A	2.90	3.10	C3	0.05	0.15
A1	0.20	0.30	D	1.00REF	
A2	0.65 TYP		D1	0.50	0.70
A3	0.36	0.46	R1	0.15TYP	
B	4.30	4.50	R2	0.15TYP	
B1	6.30	6.50	θ1	12° TYP4	
C	0.95	1.05	θ2	12° TYP4	
C1	0.127 TYP		θ3	0° ~ 7°	
C2	0.39	0.49			



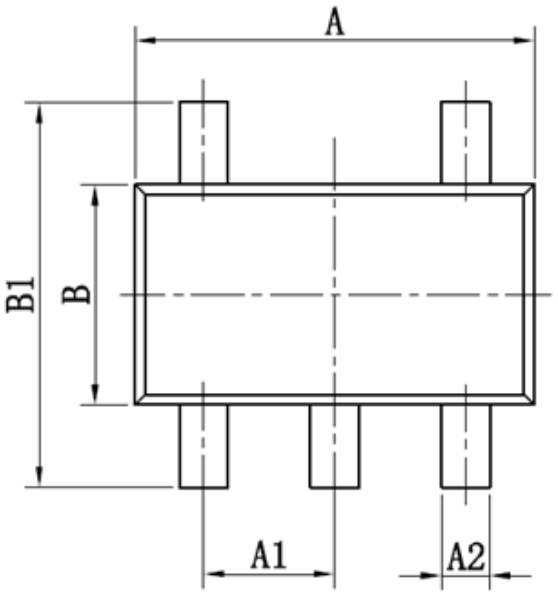
7.4 5-lead SOT23-5

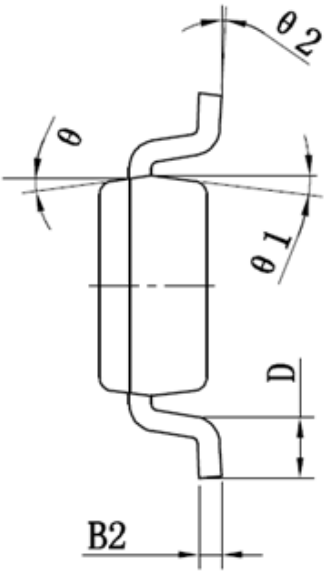
size / symbol	min(mm)	max(mm)		min(mm)	max(mm)
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

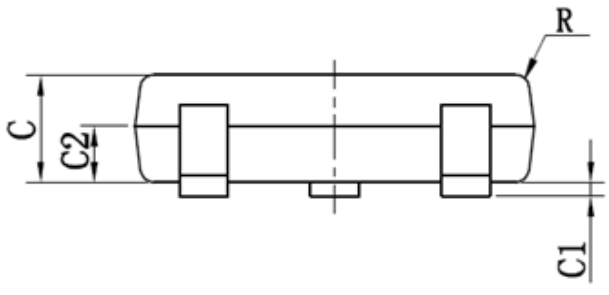


7.5 5-lead TSOT23-5

size / symbol	min(mm)	max(mm)	size / symbol	min(mm)	max(mm)
A	2.820	3.020	C1	0.000	0.100
A1	0.950(BSC)		C2	0.378	0.438
A2	0.350	0.500	D	0.300	0.600
B	1.600	1.700	θ	9° TYP4	
B1	2.650	2.950	θ1	10° TYP4	
B2	0.080	0.200	θ2	0~8°	
C	0.700	0.800			

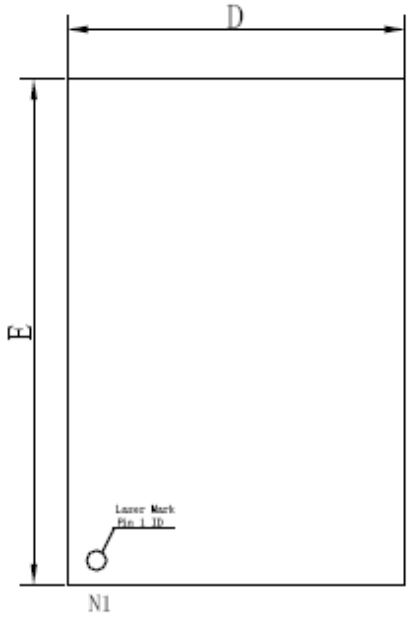


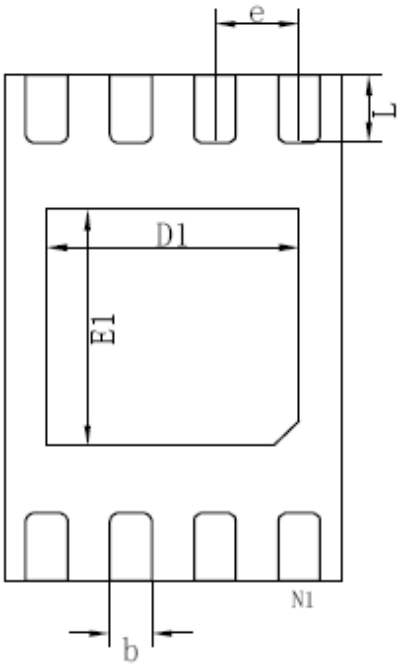


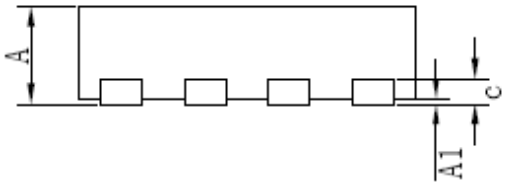


7.6 8-lead UDFN

Symbol \ size	min(mm)	typ(mm)	max(mm)	symbol \ size	min(mm)	typ(mm)	max(mm)
A	0.50	0.55	0.60	e		0.50TYP	
A1	0.00	0.03	0.05	E	2.90	3.00	3.05
b	0.20	0.25	0.30	E1	1.30	1.40	1.50
c		0.152REF		D1	1.40	1.50	1.60
D	1.90	2.00	2.05	L	0.30	0.40	0.50







8. Revision History

Version	Content	Date
V1.0	Initial Release	2021-04-06