TH24C64UB

Ultra Low Power, 64K-bit

I2C-Compatible Serial EEPROM Datasheet

Apr, 2021

V1.1

Performance Highlight

- *Wide Power Supply Range from 1.7V to 5.5V*
- *Ultra Low Power consumption for Read and Program*
- *High ESD Protection and Latch up Capability*
- *High reliability with 1000K cycling and 100 Years data retention*

Contents

General Description

The TH24C64UB is a 64-Kbit I2C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. The device is organized as 8192 × 8bits memory array with 32- byte per page. TH24C64UB provides the following features for different application.

Features

Compatible with I2C bus modes
- ✧ 1 MHz clock from 2.5V to 5.5V
- ✧ 400KHz clock from 1.7V to 2.5V

Wide Supply Voltage and temperature
- ✧ operating voltage from 1.7V to 5.5V
- ✧ operating temperature from -40 °C to 85 °C

Low power CMOS technology
- ✧ Read current 400μA, maximum
- ✧ Write current 2mA, maximum

Schmitt Trigger, Filtered Inputs for Noise Suppression

Memory array
- ✧ 64 Kbits (8 Kbytes) of EEPROM
- ✧ Page size: 32 bytes
- ✧ Additional Write Lockable Page and 128-bit Serial Number

Sequential & Random Read Features

Page Write Mode, Partial Page Writes Allowed

Software Write Protection (SWP) for Programmable Block
- ✧ Upper quarter memory array
- ✧ Upper half memory array
- ✧ Upper 3/4 memory array
- ✧ Whole memory array

Software Programmable Device Select Code

Self-timed Write Cycle (5ms maximum)

High Reliability
- ✧ Endurance: 1 Million Write Cycles
- ✧ Data Retention: 100 Years
- ✧ ESD Protection (HBM): +/- 5KV
- ✧ Latch up Capability: +/- 200mA (25°C and 125°C)

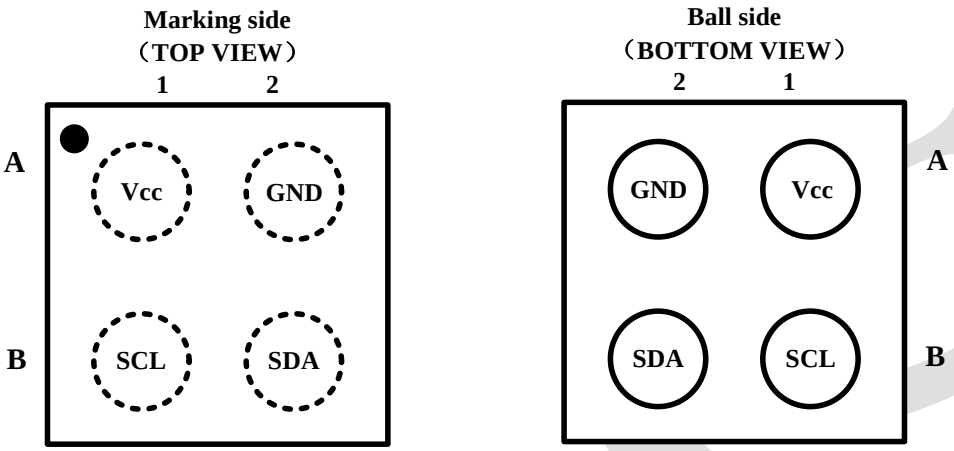
Package:

4-balls WLCSP. Ball Pitch 400um * 400um

1. Pin Configuration

1.1 Pin Configuration

Figure 1-1 WLCSP-4Balls (Ball pitch 400um * 400um)



1.2 Pin Definition

Table 1-1 Pin Definition for 4balls WLCSP Packages

Pin	Name	Type	Description
1	Vcc	Power	Power Supply
2	GND	Ground	Ground
3	SDA	I/O	Serial Data Input and Serial Data Output
4	SCL	Input	Serial Clock Input

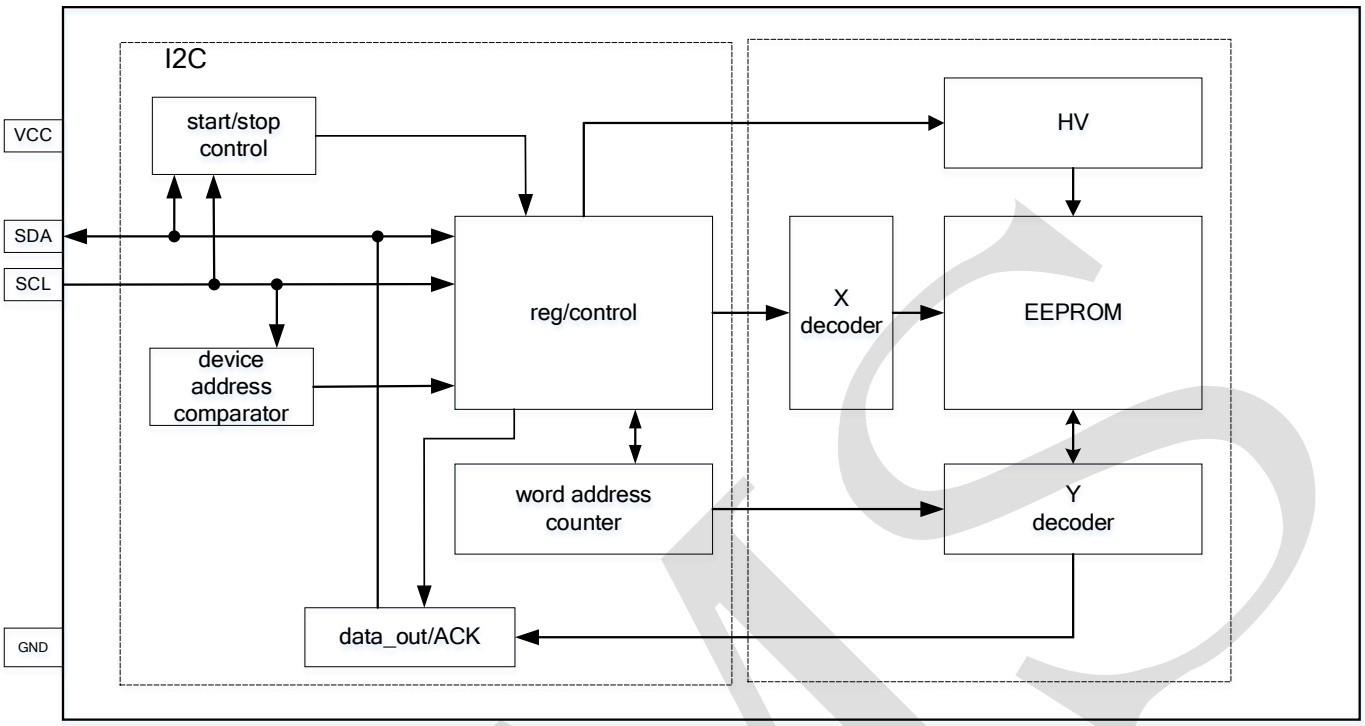
1.3 Pin Descriptions

Serial Clock (SCL): The SCL is input pin. It is used to clock in data at positive edge and clock out data from EEPROM at negative edge.

Serial Data (SDA): The SDA is bidirectional for serial data transfer. This pin is open drain driven and may be wired AND with any number of other open-drain or open-collector devices. The SDA requires a pull-up device connected to the power supply.

2. Block Diagram

Figure 2-1 Block Diagram



3. Electrical Characteristics

Table 3-1 Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Units
T	Operation Temperature	-40	85	°C
T_{STG}	Storage Temperature	-55	150	°C
V_M	Maximum Operation Voltage	-0.3	5.8	V
I_{OLM}	DC Output Current		5	mA

NOTICE: Stressing the device outside the ratings listed in Table 3-1 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3-2 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$=GND
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN}=GND

Note: [1] Test Conditions: T_A = 25°C, Freq. = 1MHz, Vcc =5.5V.

Table 3-3 DC Characteristics （Unless otherwise specified, Vcc = 1.7V to 5.5V, T_A = –40°C to 85°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
Vcc	Supply Voltage	1.7	-	5.5	V	
Isb	Standby Current		2.5	15	μA	Vcc = 5.5V
I_{CC1}	Supply Current	-	0.2	0.4	mA	Vcc = 5.5V, Read at 400Khz
I_{CC2}	Supply Current	-	1.0	2.0	mA	Vcc = 5.5V Write at 400Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = Vcc or GND
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = Vcc or GND
V_{IL}	Input Low Level	–0.6	-	0.3Vcc	V	
V_{IH}	Input High Level	0.7Vcc	-	Vcc+0.5	V	
V_{OL1}	Output Low Level Vcc = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level Vcc = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

Table 3-4 AC Characteristics （Unless otherwise specified, Vcc = 1.7V to 5.5V, T_A = –40°C to 85°C, C_L=100pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤Vcc<2.5			2.5≤Vcc≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.5	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.4	μs
t_I	Noise Suppression Time	-	-	0.08	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	START Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	START Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	STOP Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- R_L (connects to Vcc): 1.3kΩ (2.5V, 5.5V), 4kΩ (1.7V)
- Input pulse voltages: 0.3 Vcc to 0.7 Vcc
- Input rise and fall times: ≤50ns
- Input and output timing reference voltages: 0.5Vcc

Table 3-5 Reliability Characteristics [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C/ 85°C, 5.5V, Page mode

Figure 3-1 Bus Timing

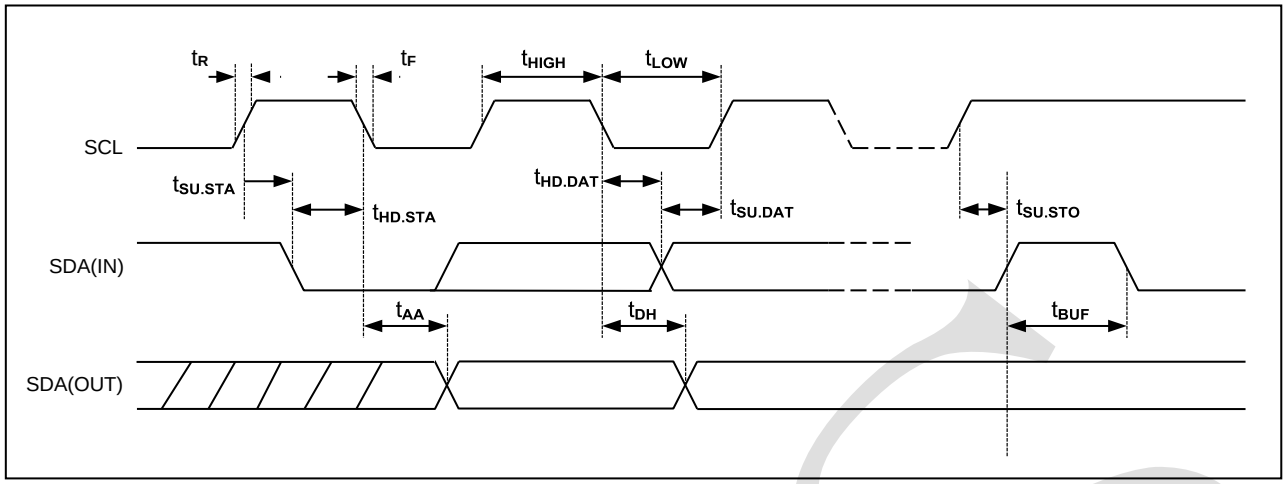
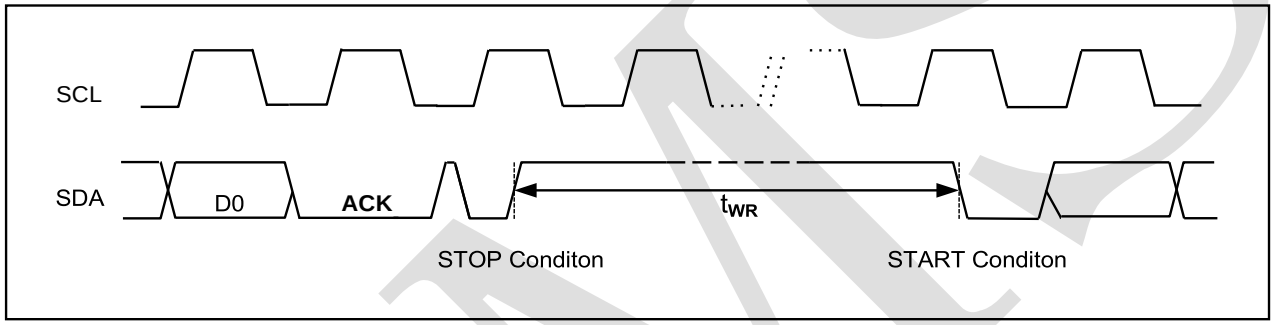


Figure 3-2 Write Cycle Timing



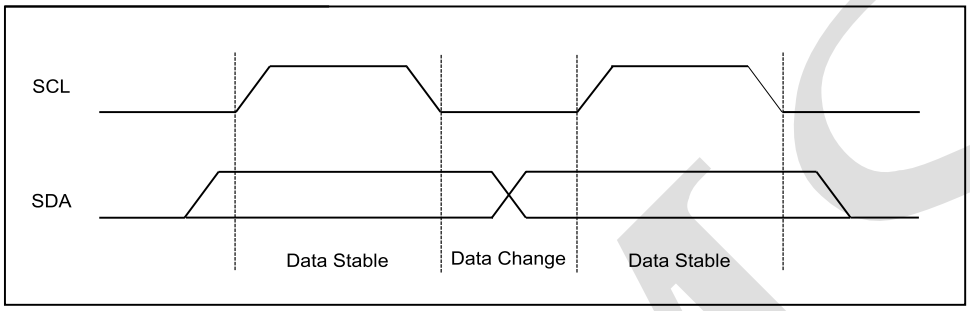
Note: [1] The write cycle time t_{WR} is the time from a valid STOP condition of a write sequence to the end of the internal clear/write cycle.

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high by an external device. Data on the SDA pin may change only during SCL low period (Refer to Figure 4-1). Data changes during SCL high period will indicate a START or STOP condition as defined below.

Figure 4-1 Data Validity



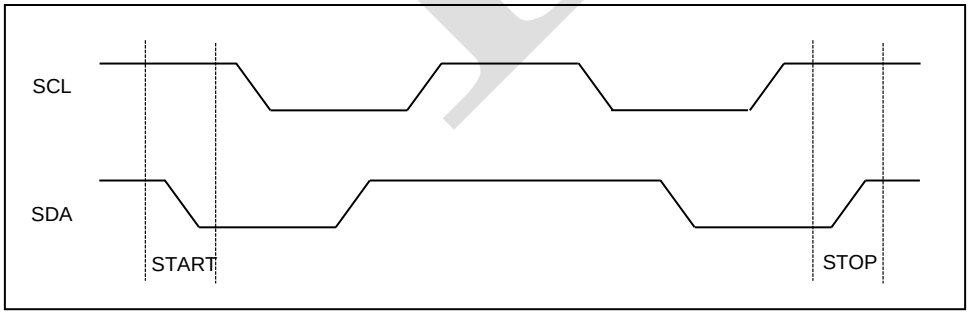
4.2 START Condition

A high-to-low transition on SDA while SCL high is a START condition, the START condition must precede any other command bits. (Refer to Figure 4-2).

4.3 STOP Condition

A low-to-high transition of SDA with SCL high is a STOP condition. After a read sequence, the STOP bit will place the TH24C64UB in a standby mode (Refer to Figure 4-2).

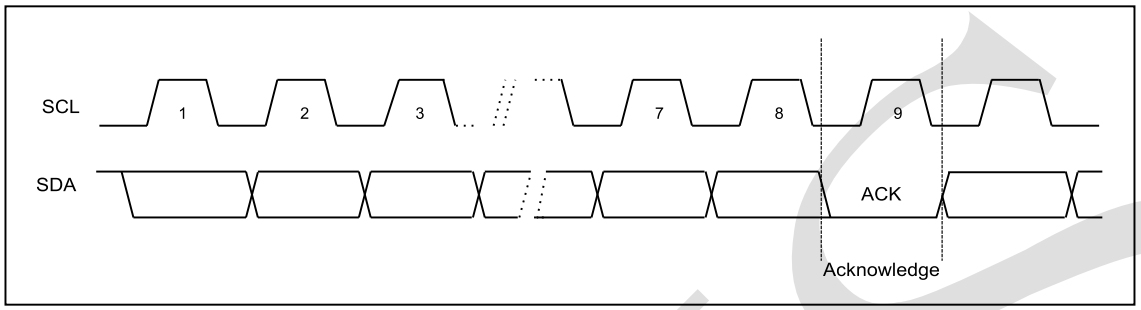
Figure 4-2 START and STOP Definition



4.4 Acknowledge (ACK)and Not Acknowledge (NoACK)

All addresses and data should be serially transmitted to and from the TH24C64UB by byte. Each byte must be 8-bit long. The TH24C64UB sends a “0” to acknowledge (ACK) that it has received each data. An ACK means SDA pull down during the ninth clock cycle. A NoACK means SDA pull up during the ninth clock cycle.

Figure 4-3 Acknowledge Bit Definition



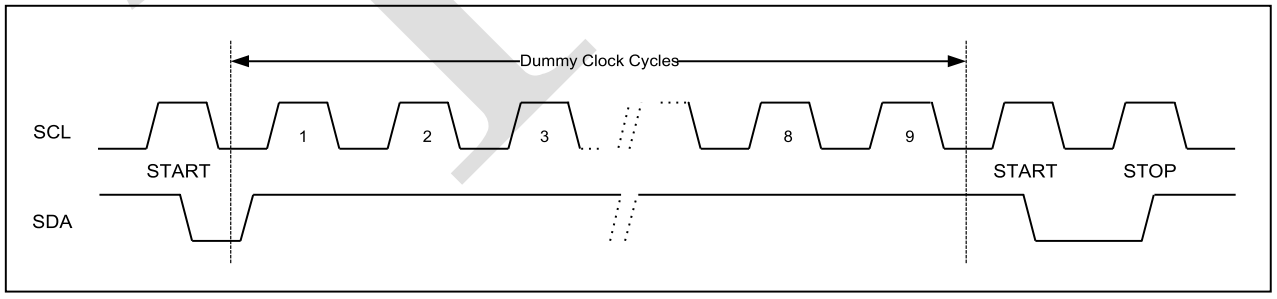
4.5 Standby Mode

The TH24C64UB features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP condition in read mode, and (c) after completing a self-time internal programming operation.

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, the device can be reset by following steps: (a) Create a START condition, (b) Clock in nine data bits “1”, and (c) create another START condition followed by a STOP condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.7 Device Address

The TH24C64UB requires an 8-bit device address after a START condition to enable the chip, the 8-bit device address consists of a 4-bit device type identifier and a 3-bit Device Select Code (DSC2, DSC1, DSC0). Refer to table below:

Table 4-1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH24C64UB	Normal Area	1	0	1	0	DSC2	DSC1	DSC0	R/W
	ID Page	1	0	1	1	DSC2	DSC1	DSC0	R/W
	Lock Bit	1	0	1	1	DSC2	DSC1	DSC0	R/W
	DSC	1	0	1	1	DSC2	DSC1	DSC0	R/W
	Serial Number	1	0	1	1	DSC2	DSC1	DSC0	1
	SWP	1	0	1	0	DSC2	DSC1	DSC0	R/W

Table 4-2 Word Address0

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH24C64UB	Normal Area	X	X	X	A12	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	0	1	X	X
	DSC	X	X	X	X	1	1	X	X
	Serial Number	X	X	X	X	1	0	X	X
	SWP	1	X	X	X	X	X	X	X

Table 4-3 Word Address1

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH24C64UB	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	X	X	A5	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	DSC	X	X	X	X	X	X	X	X
	Serial Number	X	X	X	X	A3	A2	A1	A0
	SWP	X	X	X	X	X	X	X	X

The Device Select Code DSC2/DSC1/DSC0 are software programmable by DSC register writing. The bit0 of the device address is the read/write operation selection bit. If bit0 is high, a read operation is initiated, if bit0 is low, a write operation is initiated. Upon a matched comparison result, the device will output a ACK. If not, the device will return to a standby state.

4.8 Data Security

TH24C64UB has a software data protection scheme. Users can protect the whole chip or blocks by Soft Write Protection. Please refer to 5.1.6 for detail.

5. Instructions

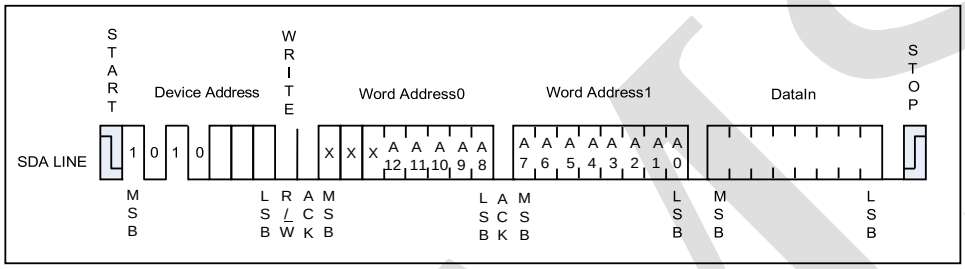
5.1 Write Operations

The read/write selection bit of Write Operations in the device address is “0”. There are two write operations: Byte Write and Page Write. In addition, Write Operations is corresponding to some utilities.

5.1.1 Byte Write

Byte write operation requires one-byte device address, two-byte word address and one-byte data in order. After receiving each byte, the device will respond an ACK. The master must terminate the write sequence with a STOP condition. And then the TH24C64UB enters an internally timed write cycle. All inputs are blocked during this write cycle and the TH24C64UB will not respond until the write is complete (Refer to Figure 5-1).

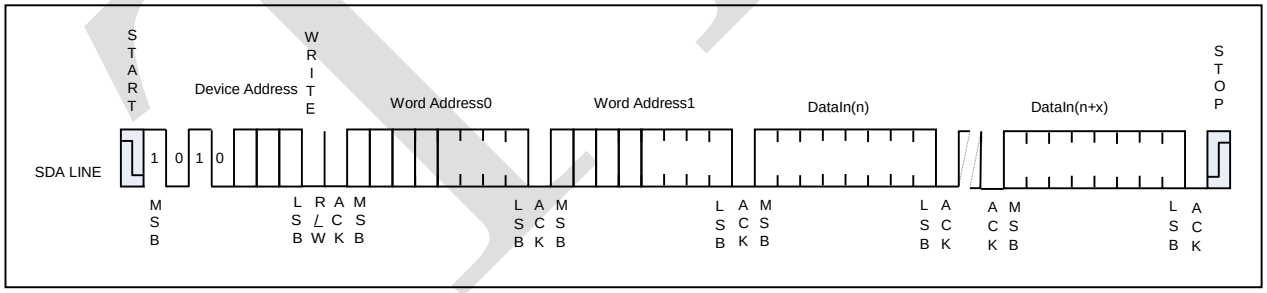
Figure 5-1 Byte Write



5.1.2 Page Write

Page write performs a similar way to Byte Write. The difference is that Page Write will not generate a STOP condition after clock in the first byte. Instead, after the TH24C64UB acknowledges receipt of the first byte data, the master can transmit more data continuously. The TH24C64UB will respond with a “0” after each data byte received. The master must terminate the page write sequence with a STOP condition (Refer to Figure 5-2).

Figure 5-2 Page Write



The lowest five bits of the word address are internally incremented by one. The higher word address bits stay constant, retain the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 bytes data are transmitted to the TH24C64UB, the word address will roll-over and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started, the TH24C64UB inputs are blocked, will not respond any ACK. To find out whether this cycle is over, Acknowledge Polling could be used. This involves sending a START condition followed by the device address. The read/write bit is representative of the desired operation. Until the internal write cycle has completed, TH24C64UB will response “0”, allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (refer to 5.1.2), except for the following differences:

- Device type identifier = 1011b
- Address bits A11/A10 must be ‘00’.
- Address bits A4~A0 define the byte address inside the Identification page.
- Other Address bits are don’t care.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.1.5 Lock Identification Page

The Lock Identification Page (Lock ID) instruction permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (refer to 5.1.1), except for the following differences:

- Device type identifier = 1011b
- Address bit A11A10 must be ‘01’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxxxx1x, where x is don’t care

5.1.6 Soft Write Protection

By writing specific values in a register (Table 5-1) located at address 1xxx_xxxx_xxxx_xxxxb,

- device type identifier = 1010b

the memory array can be write-protected by blocks, which size can be defined as:

- the upper quarter memory array
- the upper half memory array
- the upper 3/4 memory array
- the whole memory array

Writing in the Soft Write Protect (SWP) register is performed with a Byte Write instruction at address 1xxx_xxxx_xxxx_xxxxb. Bit 7~5 of the data byte are not significant (Don't Care). Writing more than one byte will discard the write cycle (Write protect register content will not be changed).

Figure 5-3 Soft Write Protection

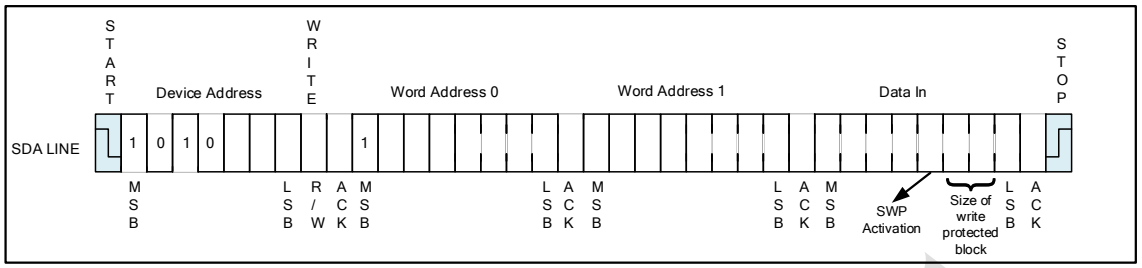


Table 5-1 SWP Register

Bit	7	6	5	4	3	2	1	0	Default
Bit Definition	-	-	-	-	Write protect activation	Size of write protected block		-	/
R/W	RO	RO	RO	RO	RW	RW	RW	RW	/
Default	0	0	0	0	0	0	0	0	00H

Table 5-2 Bit Definition for SWP Register

Bit	Definition	Description	Defaults	Note
7~4	/	Reserved for future use	0000	/
3	Write protect activation	Enables or disables the Soft Write Protection 0: the whole memory can be written 1: the concerned block is write-protected	0	/
2~1	Size of write protected block	Define the size of the memory block to be protected 00: the upper quarter of memory is write-protected 01: the upper half memory is write-protected 10: the upper 3/4 of memory is write-protected 11: the whole memory is write-protected	00	00
0	/	Reserved for future use	0	/

Table5-3 Range of Protected Area Address

SWP BLOCK	Description	Protected Area Address (Hex)
00b(default)	The upper quarter of memory is write-protected	1800~1FFF
01b	The upper half memory is write-protected	1000~1FFF
10b	The upper 3/4 of memory are write-protected	0800~1FFF
11b	The whole memory is write-protected	0000~1FFF

5.1.7 DSC Register Write Command

The Device Select Code (DSC) is software programmable by the DSC Register Write Command, it is an instruction similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A11A10 must be '11', all other address bits are don't care.

If a lock ID page command is sent, both the ID page and DSC Register is locked. The DSC[2:0] register is then frozen.

Figure 5-4 DSC Register Write

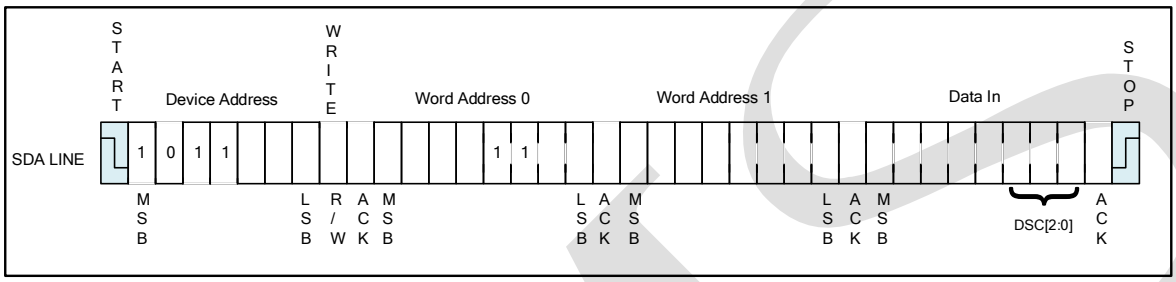


Table5-4 DSC Register

Bit	7	6	5	4	3	2	1	0	Default
Bit Definition	-	-	-	-	-	DSC[2:0]			/
R/W	RO	RO	RO	RO	RO	RW	RW	RW	/
Default	0	0	0	0	0	0	0	0	00H

Table 5-5 Bit Definition for DSC Register

Bit	Definition	Description	Defaults	Note
7~3	/	Reserved for future use	00000	/
2~0	DSC[2:0]	The Device Address of the EEPROM is constructed as {1011/1010, DSC[2:0], R/W } DSC[2:0] is defined as Device Select Code.	000	/

5.2 Read Operations

Read operations are initiated in the same way as write operations, except the read/write selection bit in the device address is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

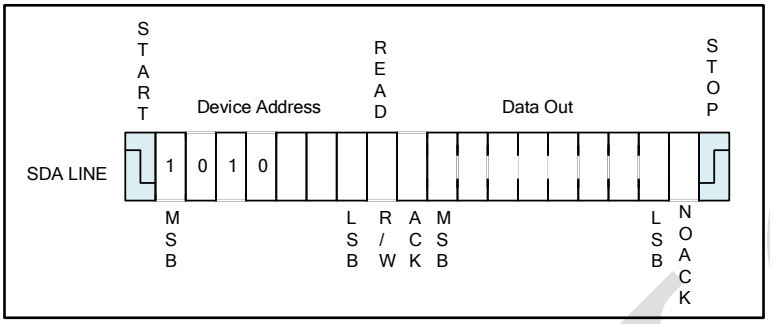
5.2.1 Current Address Read

If the power is stay valid, After the STOP condition of the last command, the last address accessed during the

last read or write operation is always incremented by one, For the Current Address Read operation, following a START condition, the bus master only sends device address with the R/W selection bit 1. The device acknowledges this, the data at the current address (the last address accessed during the last read or write operation incremented by one) is serially clocked out. The master can send a NoACK and a STOP condition to terminate the Current Address Read. (Refer to Figure 5-5).

If the last byte of the last memory page is reached, the address counter rolls over to the first byte of the first page.

Figure 5-5 Current Address Read

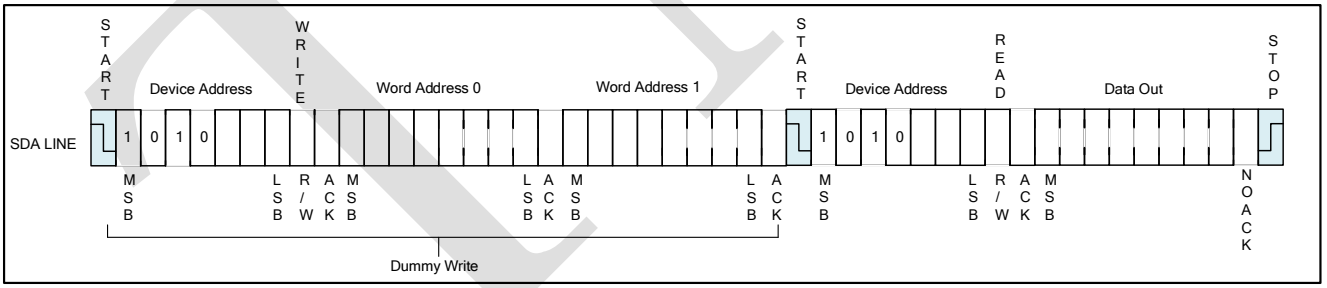


5.2.2 Random Read

The Random Address Read is a sequence composed of a truncated Write sequence (to define a new address pointer value) followed by a current Read.

The Random Address Read sequence is therefore the sum of [START + Device Address with R/W=0 + two address bytes] (without STOP condition) and [START + Device Address with R/W=1]. The memory device acknowledges the sequence and then outputs the contents of the addressed byte. To terminate the data transfer, the bus master does not acknowledge the last data byte and then issues a STOP condition. (Refer to Figure 5-6).

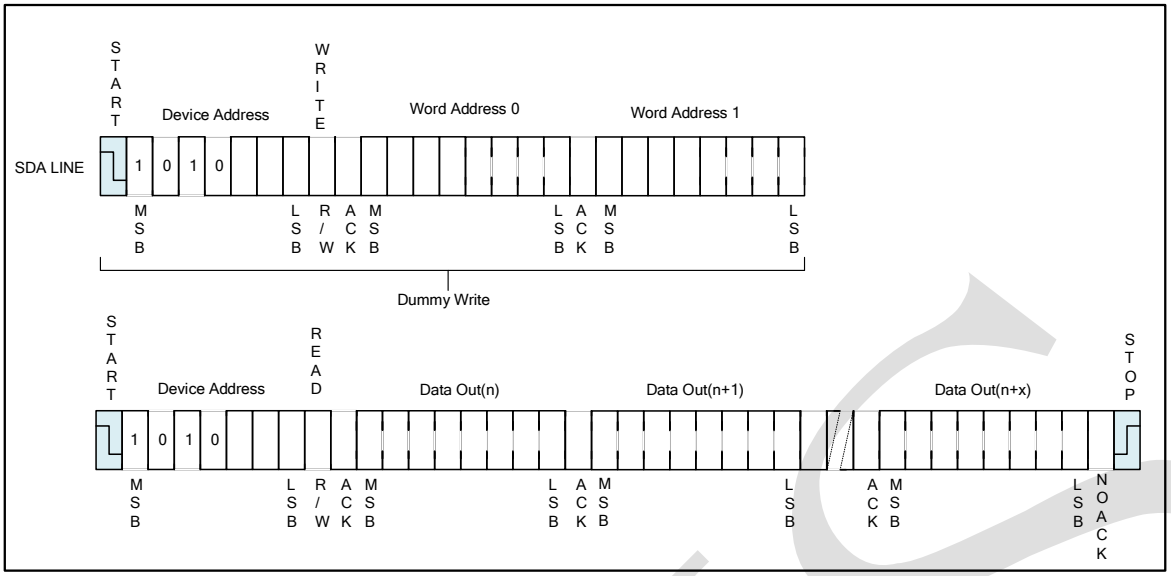
Figure 5-6 Random Read



5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the master receives a byte data, it responds with an ACK. As long as the device receives ACK, it will continue to increment the word address and serially clock out the reading data. When the memory address boundary is reached, the word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the master does not respond with a “0” and following a STOP condition. (Refer to Figure 5-7)

Figure 5-7 Sequential Read



5.2.4 Read Identification Page

The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (refer to 5.2.3), except for the following differences:

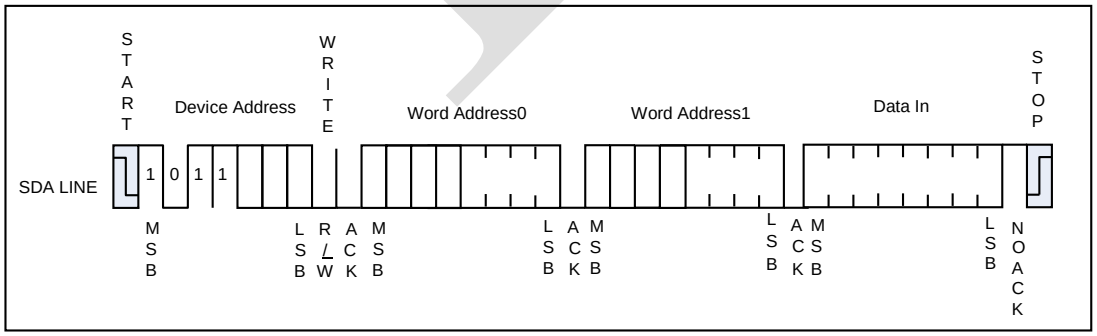
- Device type identifier = 1011b.
- The word address bits A11 and A10 must be 0.
- The LSB address bits A4~A0 define the byte address inside the Identification Page.

The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 28d, the number of bytes should be less than or equal to 4, as the ID page boundary is 32 bytes).

5.2.5 Read the Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific command sequence [Identification Page Write instruction + one data byte] to the device. The device returns an ACK if the Identification page is unlocked or a NoACK if the Identification page is locked. (Refer to Figure 5-8)

Figure 5-8 Lock Status Read (When Identification page locked, return No-ACK after the data-in)



5.2.6 Read Serial Number

The serial number is an additional unique 128 bits which can be read only.

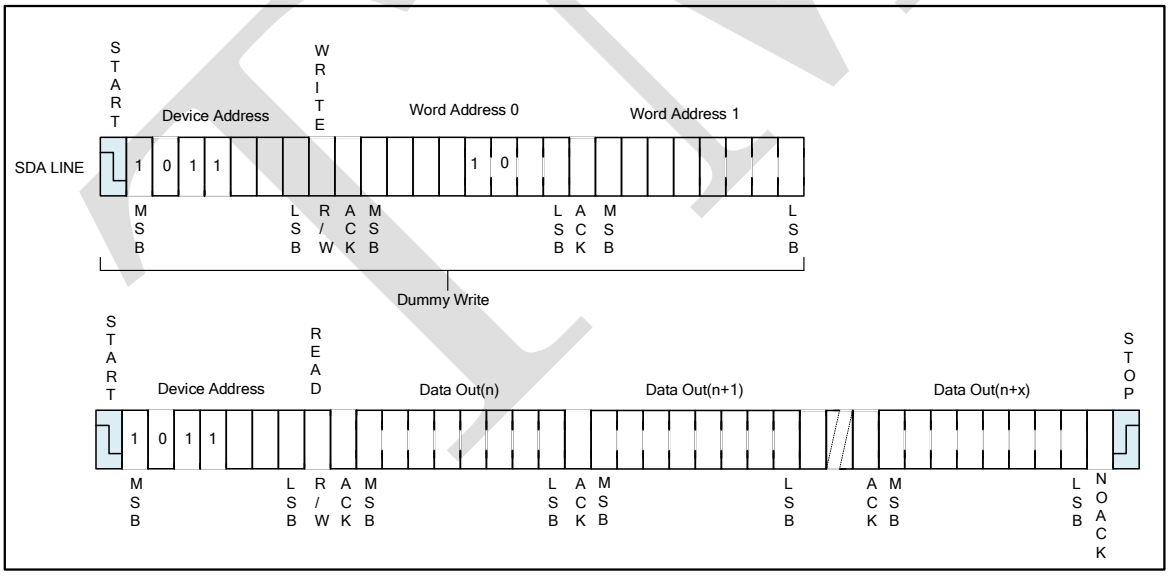
Reading the serial number is similar to the sequential read scheme, but the device address must follow Table 4-1, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number region to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number region, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one.

Additionally, bit A11 and A10 of Word Address must be '10', refer to the Table 4-2. If a Word Address other than '10' is used, then the device will output undefined data.
Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

When the end of the 128-bit serial number is reached (16 bytes of data), continue reading the extended memory region will result in a repeated 16 bytes data. Upon reaching the end of the 16-byte extended memory region, the word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the master does not respond with a zero (ACK) and instead issues a STOP condition (Refer to Figure 5-9)

Figure 5-9 Read Serial Number



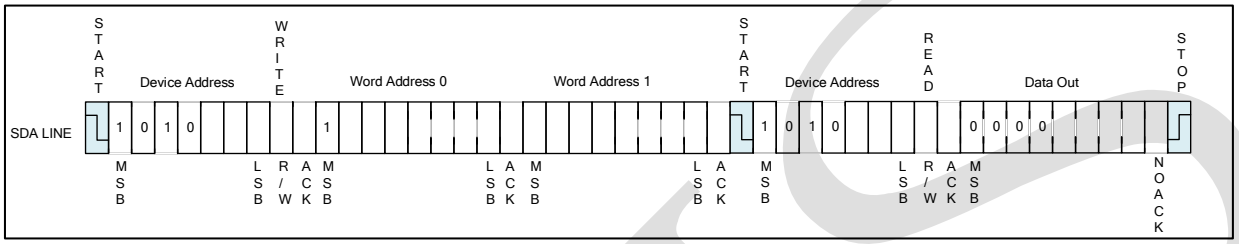
5.2.7 Read the Soft Write Protect register

Reading the Soft Write Protect register is performed with a Random Read instruction at address 1xxx_xxxx_xxxx_xxxxb.

Bit 7~4 of the Soft Write Protect register content are read as 4'b0000.

The signification of the Protect Register lower bit 3~0 are defined in Section 5.1.6. Reading more than one byte will loop on reading the Soft Write Protect Register value. The Soft Write Protect register cannot be read while a write cycle (tw) is ongoing.

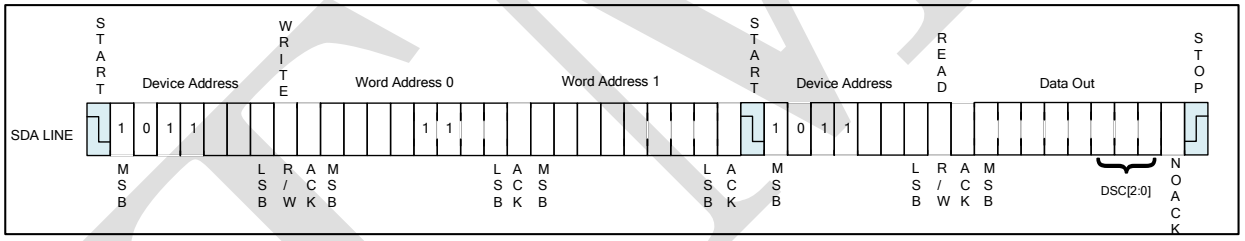
Figure 5-10 SWP register Read



5.2.8 Read the DSC register

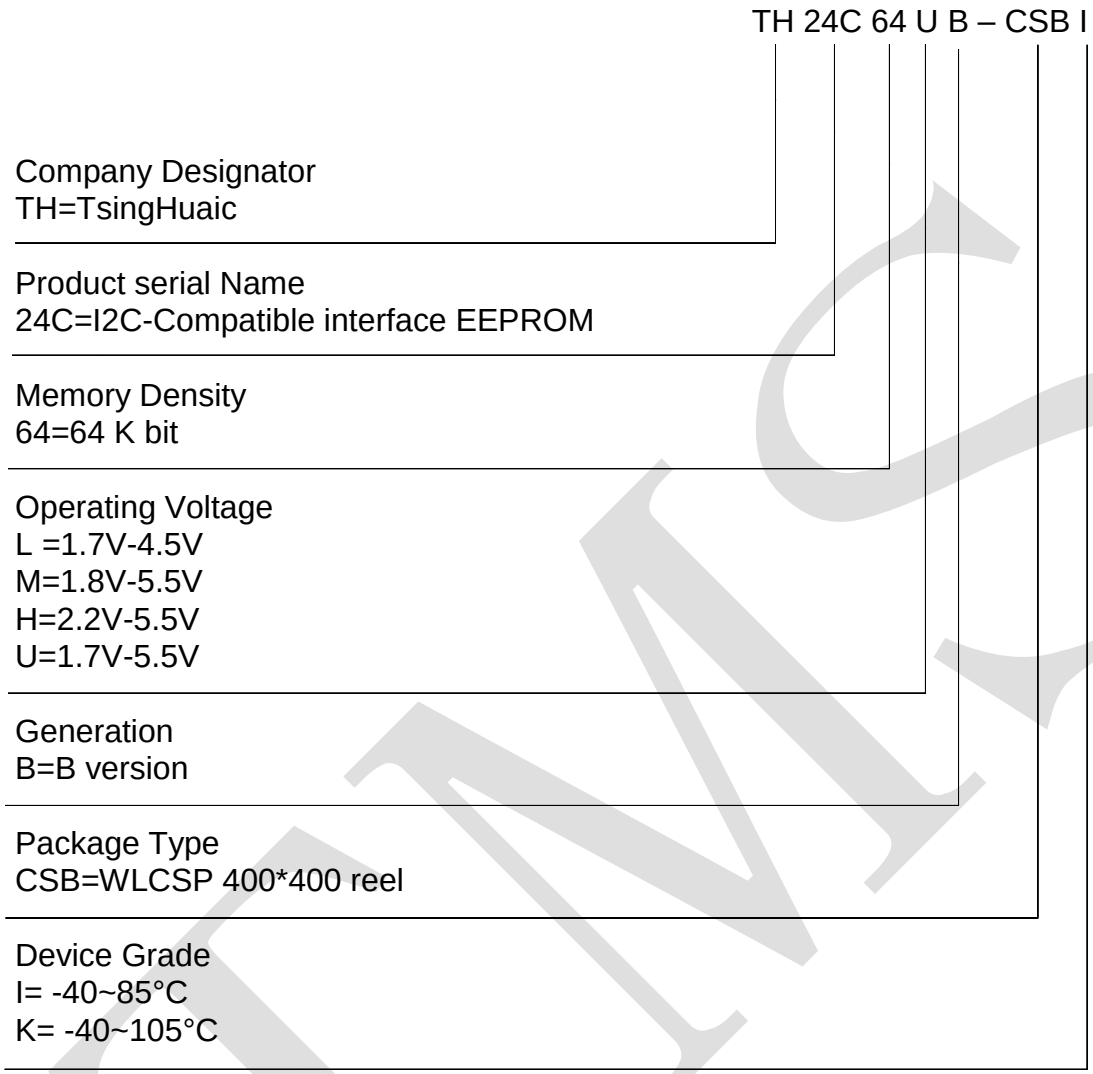
Reading the DSC[2:0] register is performed with a Random Read instruction with device identifier "1011b" and Word Address bit A11/A10 are 11b. The 3 LSB of the output data is expected to be the same with the Device Select Code in Device address.

Figure 5-11 DSC register Read



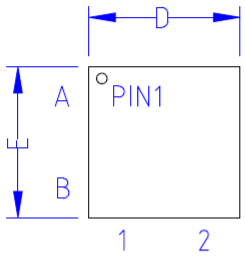
6. Ordering Code Detail

Example:

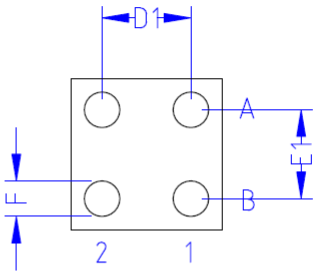


7. Package information

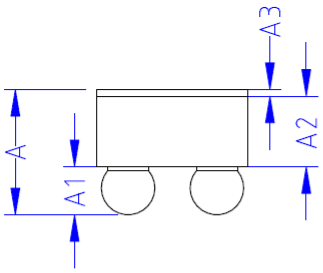
7.1 4BALL-WLCSP(400um*400um)



TOP VIEW
Ball Down



BOTTOM VIEW
Ball Up



SIDE VIEW

Unit:mm

		NO.	Mean	Tolerance
Top Thickness		A	0.280	±0.0275
Ball Height+UBM Thickness		A1	0.055	±0.010
Wafer/Grinding Thickness		A2	0.2	±0.0125
Backside Coating Thickness		A3	0.025	±0.005
Pkg Die Size	X	D	0.661	±0.025
	Y	E	0.662	±0.025
Ball Size afer reflow		F	0.160	±0.080
Ball Pitch		D1	0.400	NA
		D2	0.400	NA
		E1	0.400	NA
		E2	0.400	NA

Notch

Revision History

Version	Content	Date
V1.1	Initial Release	2021-04-06
V1.2	Change Ordering Code Detail	2022-01-21